

74HC164; 74HCT164

8-bit serial-in, parallel-out shift register

Rev. 03 — 4 April 2005

Product data sheet

1. General description

The 74HC164; 74HCT164 are high-speed Si-gate CMOS devices and are pin compatible with Low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC164; 74HCT164 are 8-bit edge-triggered shift registers with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (DSA or DSB); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock (CP) input and enters into Q0, which is the logical AND of the two data inputs (DSA and DSB) that existed one set-up time prior to the rising clock edge.

A LOW level on the master reset ($\overline{\text{MR}}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

2. Features

- Gated serial data inputs
- Asynchronous master reset
- Complies with JEDEC standard no. 7A
- ESD protection:
 - ◆ HBM EIA/JESD22-A114-B exceeds 2000 V
 - ◆ MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$.

3. Quick reference data

Table 1: Quick reference data
 $GND = 0\text{ V}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Type 74HC164						
t_{PHL} , t_{PLH}	propagation delay					
	CP to Qn	$C_L = 15\text{ pF}$; $V_{\text{CC}} = 5\text{ V}$	-	12	-	ns
	$\overline{\text{MR}}$ to Qn	$C_L = 15\text{ pF}$; $V_{\text{CC}} = 5\text{ V}$	-	11	-	ns

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Table 1: Quick reference data ...continued

$GND = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; $t_r = t_f = 6\text{ ns}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{max}	maximum clock frequency	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	-	78	-	MHz
C_I	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance per package		[1]	40	-	pF
Type 74HCT164						
t_{PHL}, t_{PLH}	propagation delay					
	CP to Qn	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	-	14	-	ns
	\overline{MR} to Qn	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	-	16	-	ns
f_{max}	maximum clock frequency	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	-	61	-	MHz
C_I	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance per package		[1]	40	-	pF
			[3]			

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

N = number of inputs switching

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

[2] For HC the condition is $V_I = GND$ to V_{CC} .

[3] For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5\text{ V}$.

4. Ordering information

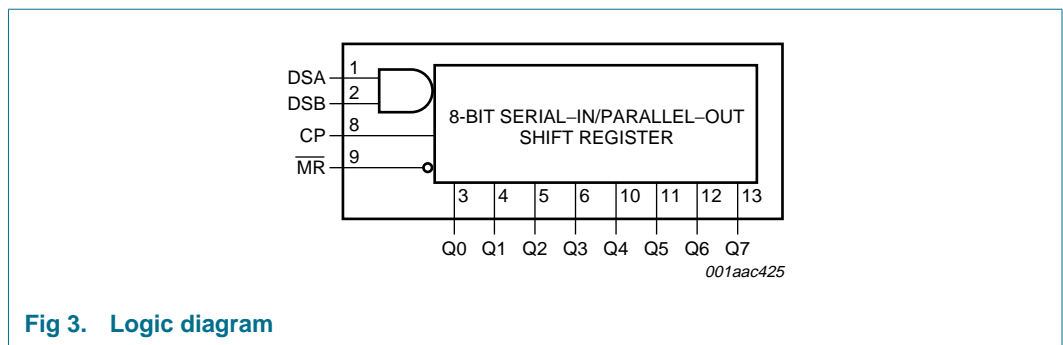
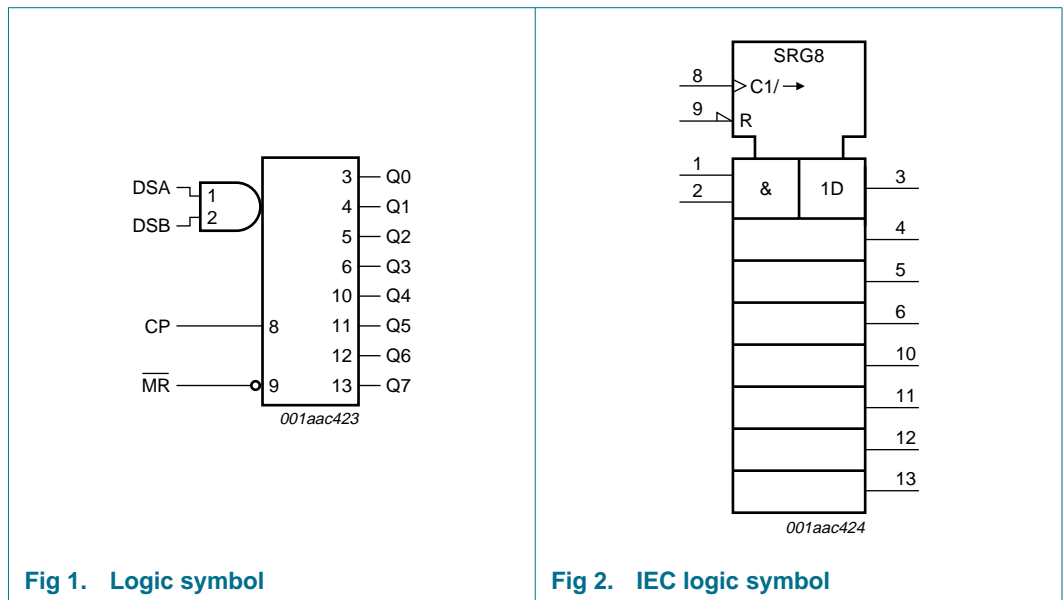
Table 2: Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC164N	-40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HC164D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm; body thickness 1.47 mm	SOT108-2
74HC164DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HC164PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT164N	-40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HCT164D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm; body thickness 1.47 mm	SOT108-2

Table 2: Ordering information ...continued

Type number	Package			Version
	Temperature range	Name	Description	
74HCT164DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCT164PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT164BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

5. Functional diagram



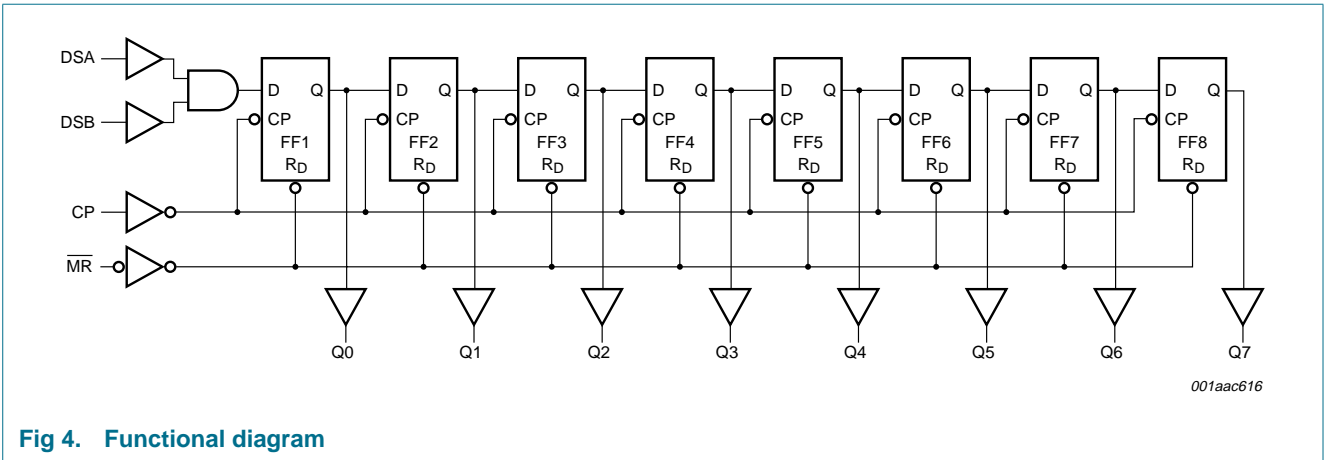


Fig 4. Functional diagram

6. Pinning information

6.1 Pinning

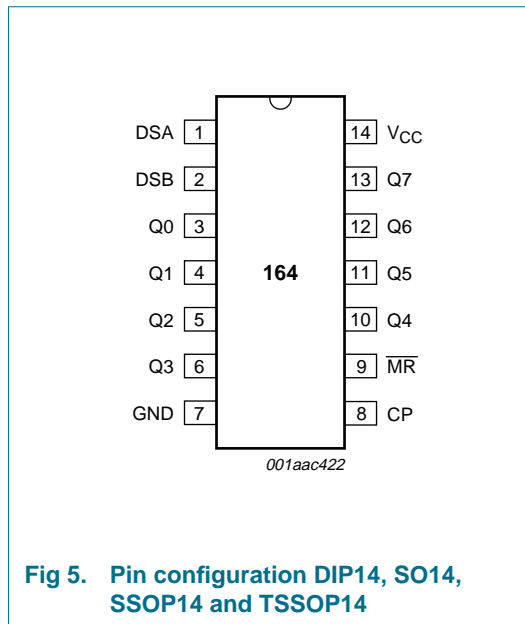


Fig 5. Pin configuration DIP14, SO14, SSOP14 and TSSOP14

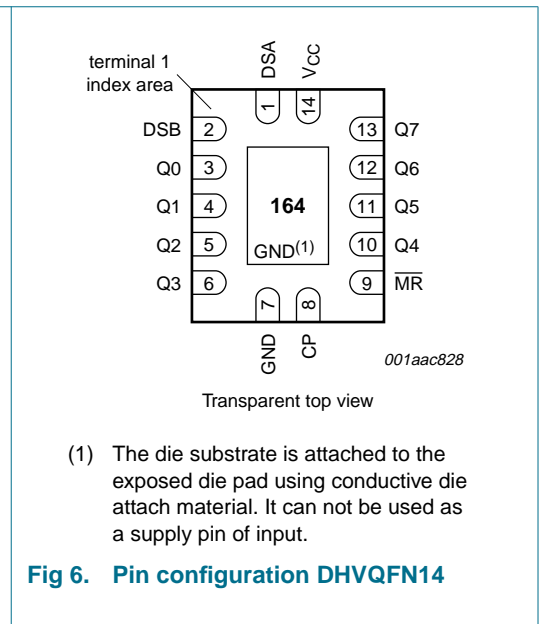


Fig 6. Pin configuration DHVQFN14

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
DSA	1	data input
DSB	2	data input
Q0	3	output
Q1	4	output
Q2	5	output
Q3	6	output

Table 3: Pin description ...continued

Symbol	Pin	Description
GND	7	ground (0 V)
CP	8	clock input (LOW-to-HIGH, edge-triggered)
$\overline{\text{MR}}$	9	master reset input (active LOW)
Q4	10	output
Q5	11	output
Q6	12	output
Q7	13	output
V _{CC}	14	positive supply voltage

7. Functional description

7.1 Function selection

Table 4: Function table [1]

Operating modes	Input				Output	
	$\overline{\text{MR}}$	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
	H	↑	l	h	L	q0 to q6
	H	↑	h	l	L	q0 to q6
	H	↑	h	h	H	q0 to q6

[1] H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

q = lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition

↑ = LOW-to-HIGH clock transition

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input diode current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output diode current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output source or sink current	V _O = -0.5 V to V _{CC} + 0.5 V	-	±25	mA
I _{CC} , I _{GND}	V _{CC} or GND current		-	±50	mA
T _{stg}	storage temperature		-65	+150	°C

Table 5: Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
P _{tot}	total power dissipation				
	DIP14 package		[1] -	750	mW
	SO14; SSOP14; TSSOP14; DHVQFN14 package		[2] -	500	mW

[1] For DIP14 packages: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO14 packages: P_{tot} derates linearly with 8 mW/K above 70 °C.

For SSOP14 and TSSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Type 74HC164						
V _{CC}	supply voltage		2.0	5.0	6.0	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
t _r , t _f	input rise and fall time	V _{CC} = 2.0 V	-	-	1000	ns
		V _{CC} = 4.5 V	-	6.0	500	ns
		V _{CC} = 6.0 V	-	-	400	ns
T _{amb}	ambient temperature		-40	-	+125	°C
Type 74HCT164						
V _{CC}	supply voltage		4.5	5.0	6.0	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
t _r , t _f	input rise and fall time	V _{CC} = 4.5 V	-	6.0	500	ns
T _{amb}	ambient temperature		-40	-	+125	°C

10. Static characteristics

Table 7: Static characteristics for 74HC164

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	V

Table 7: Static characteristics for 74HC164 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.98	4.32	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	0.15	0.26	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	μA
			I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-
C _I	input capacitance		-	3.5	-	pF
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	-	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	-	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	-	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.84	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	-	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	μA
			I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-

Table 7: Static characteristics for 74HC164 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}	-	-	-	
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	-	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	-	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	-	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.7	-	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.2	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}	-	-	-	
		I _O = 20 μA; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	-	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	160	μA

Table 8: Static characteristics for 74HCT164

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}	-	-	-	
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.98	4.32	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}	-	-	-	
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	0.15	0.26	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} - 2.1 V; other inputs V _I = V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A	-	100	360	μA
C _I	input capacitance		-	3.5	-	pF

Table 8: Static characteristics for 74HCT164 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40\text{ °C to }+85\text{ °C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	-	-	V
		$I_O = -4\text{ mA}; V_{CC} = 4.5\text{ V}$	3.84	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	-	-	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 4.5\text{ V}$	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}\text{ or GND}; V_{CC} = 5.5\text{ V}$	-	-	± 1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}\text{ or GND}; I_O = 0\text{ A}; V_{CC} = 5.5\text{ V}$	-	-	80.0	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC} - 2.1\text{ V};$ other inputs $V_I = V_{CC}\text{ or GND};$ $V_{CC} = 4.5\text{ V to }5.5\text{ V}; I_O = 0\text{ A}$	-	-	450	μA
$T_{amb} = -40\text{ °C to }+125\text{ °C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	-	-	V
		$I_O = -4\text{ mA}; V_{CC} = 4.5\text{ V}$	3.7	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	-	-	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 4.5\text{ V}$	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}\text{ or GND}; V_{CC} = 5.5\text{ V}$	-	-	± 1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}\text{ or GND}; I_O = 0\text{ A}; V_{CC} = 5.5\text{ V}$	-	-	160.0	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC} - 2.1\text{ V};$ other inputs $V_I = V_{CC}\text{ or GND};$ $V_{CC} = 4.5\text{ V to }5.5\text{ V}; I_O = 0\text{ A}$	-	-	490	μA

11. Dynamic characteristics

Table 9: Dynamic characteristics for 74HC164
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; test circuit see [Figure 10](#); unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
T_{amb} = 25 °C							
t _{PHL} , t _{PLH}	propagation delay CP to Qn	see Figure 7					
		V _{CC} = 2.0 V	-	41	170	ns	
		V _{CC} = 4.5 V	-	15	34	ns	
		V _{CC} = 6.0 V	-	12	29	ns	
t _{PHL}	propagation delay MR to Qn	see Figure 8					
		V _{CC} = 2.0 V	-	39	140	ns	
		V _{CC} = 4.5 V	-	14	28	ns	
		V _{CC} = 6.0 V	-	11	24	ns	
t _{THL} , t _{TLH}	output transition time	see Figure 7					
		V _{CC} = 2.0 V	-	19	75	ns	
		V _{CC} = 4.5 V	-	7	15	ns	
		V _{CC} = 6.0 V	-	6	13	ns	
t _w	clock pulse width; HIGH or LOW	see Figure 7					
		V _{CC} = 2.0 V	80	14	-	ns	
		V _{CC} = 4.5 V	16	5	-	ns	
			V _{CC} = 6.0 V	14	4	-	ns
	master reset pulse width; LOW	see Figure 8					
		V _{CC} = 2.0 V	60	17	-	ns	
V _{CC} = 4.5 V		12	6	-	ns		
		V _{CC} = 6.0 V	10	5	-	ns	
t _{rem}	removal time $\overline{\text{MR}}$ to CP	see Figure 8					
		V _{CC} = 2.0 V	60	17	-	ns	
		V _{CC} = 4.5 V	12	6	-	ns	
		V _{CC} = 6.0 V	10	5	-	ns	
t _{su}	set-up time DSA, and DSB to CP	see Figure 9					
		V _{CC} = 2.0 V	60	8	-	ns	
		V _{CC} = 4.5 V	12	3	-	ns	
		V _{CC} = 6.0 V	10	2	-	ns	
t _h	hold time DSA and DSB to CP	see Figure 9					
		V _{CC} = 2.0 V	+4	-6	-	ns	
		V _{CC} = 4.5 V	+4	-2	-	ns	
		V _{CC} = 6.0 V	+4	-2	-	ns	
f _{max}	maximum clock pulse frequency	see Figure 7					
		V _{CC} = 2.0 V	6	23	-	MHz	
		V _{CC} = 4.5 V	30	71	-	MHz	
		V _{CC} = 6.0 V	35	85	-	MHz	

Table 9: Dynamic characteristics for 74HC164 ...continued

$GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; test circuit see [Figure 10](#); unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$T_{amb} = -40\text{ °C to }+85\text{ °C}$							
t_{PHL}, t_{PLH}	propagation delay CP to Qn	see Figure 7					
		$V_{CC} = 2.0\text{ V}$	-	-	215	ns	
		$V_{CC} = 4.5\text{ V}$	-	-	43	ns	
		$V_{CC} = 6.0\text{ V}$	-	-	37	ns	
t_{PHL}	propagation delay MR to Qn	see Figure 8					
		$V_{CC} = 2.0\text{ V}$	-	-	175	ns	
		$V_{CC} = 4.5\text{ V}$	-	-	35	ns	
		$V_{CC} = 6.0\text{ V}$	-	-	30	ns	
t_{THL}, t_{TLH}	output transition time	see Figure 7					
		$V_{CC} = 2.0\text{ V}$	-	-	95	ns	
		$V_{CC} = 4.5\text{ V}$	-	-	19	ns	
		$V_{CC} = 6.0\text{ V}$	-	-	16	ns	
t_w	clock pulse width; HIGH or LOW	see Figure 7					
		$V_{CC} = 2.0\text{ V}$	100	-	-	ns	
		$V_{CC} = 4.5\text{ V}$	20	-	-	ns	
		$V_{CC} = 6.0\text{ V}$	17	-	-	ns	
		master reset pulse width; LOW	see Figure 8				
			$V_{CC} = 2.0\text{ V}$	75	-	-	ns
	$V_{CC} = 4.5\text{ V}$		15	-	-	ns	
	$V_{CC} = 6.0\text{ V}$		13	-	-	ns	
	t_{rem}	removal time \overline{MR} to CP	see Figure 8				
			$V_{CC} = 2.0\text{ V}$	75	-	-	ns
$V_{CC} = 4.5\text{ V}$			15	-	-	ns	
$V_{CC} = 6.0\text{ V}$			13	-	-	ns	
t_{su}	set-up time DSA and DSB to CP	see Figure 9					
		$V_{CC} = 2.0\text{ V}$	75	-	-	ns	
		$V_{CC} = 4.5\text{ V}$	15	-	-	ns	
		$V_{CC} = 6.0\text{ V}$	13	-	-	ns	
t_h	hold time DSA and DSB to CP	see Figure 9					
		$V_{CC} = 2.0\text{ V}$	4	-	-	ns	
		$V_{CC} = 4.5\text{ V}$	4	-	-	ns	
		$V_{CC} = 6.0\text{ V}$	4	-	-	ns	
f_{max}	maximum clock pulse frequency	see Figure 7					
		$V_{CC} = 2.0\text{ V}$	5	-	-	MHz	
		$V_{CC} = 4.5\text{ V}$	24	-	-	MHz	
		$V_{CC} = 6.0\text{ V}$	28	-	-	MHz	

Table 9: Dynamic characteristics for 74HC164 ...continued*GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; test circuit see [Figure 10](#); unless otherwise specified*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$T_{amb} = -40$ °C to $+125$ °C							
t_{PHL}, t_{PLH}	propagation delay CP to Qn	see Figure 7					
		$V_{CC} = 2.0$ V	-	-	255	ns	
		$V_{CC} = 4.5$ V	-	-	51	ns	
		$V_{CC} = 6.0$ V	-	-	43	ns	
t_{PHL}	propagation delay MR to Qn	see Figure 7					
		$V_{CC} = 2.0$ V	-	-	210	ns	
		$V_{CC} = 4.5$ V	-	-	42	ns	
		$V_{CC} = 6.0$ V	-	-	36	ns	
t_{THL}, t_{TLH}	output transition time	see Figure 7					
		$V_{CC} = 2.0$ V	-	-	110	ns	
		$V_{CC} = 4.5$ V	-	-	22	ns	
		$V_{CC} = 6.0$ V	-	-	19	ns	
t_w	clock pulse width; HIGH or LOW	see Figure 7					
		$V_{CC} = 2.0$ V	120	-	-	ns	
		$V_{CC} = 4.5$ V	24	-	-	ns	
		$V_{CC} = 6.0$ V	20	-	-	ns	
	master reset pulse width; LOW	see Figure 7					
		$V_{CC} = 2.0$ V	90	-	-	ns	
$V_{CC} = 4.5$ V		18	-	-	ns		
	$V_{CC} = 6.0$ V	15	-	-	ns		
t_{rem}	removal time \overline{MR} to CP	see Figure 8					
		$V_{CC} = 2.0$ V	90	-	-	ns	
		$V_{CC} = 4.5$ V	18	-	-	ns	
	$V_{CC} = 6.0$ V	15	-	-	ns		
t_{su}	set-up time DSA and DSB to CP	see Figure 9					
		$V_{CC} = 2.0$ V	90	-	-	ns	
		$V_{CC} = 4.5$ V	18	-	-	ns	
	$V_{CC} = 6.0$ V	15	-	-	ns		
t_h	hold time DSA and DSB to CP	see Figure 9					
		$V_{CC} = 2.0$ V	4	-	-	ns	
		$V_{CC} = 4.5$ V	4	-	-	ns	
	$V_{CC} = 6.0$ V	4	-	-	ns		
f_{max}	maximum clock pulse frequency	see Figure 7					
		$V_{CC} = 2.0$ V	4	-	-	MHz	
		$V_{CC} = 4.5$ V	20	-	-	MHz	
	$V_{CC} = 6.0$ V	24	-	-	MHz		

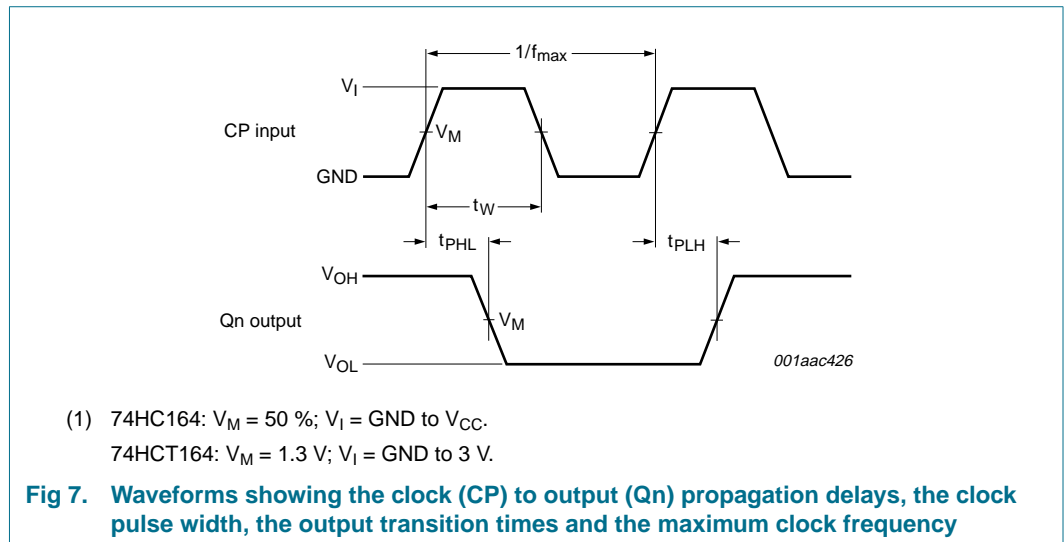
Table 10: Dynamic characteristics for 74HCT164*GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; test circuit see [Figure 10](#); unless otherwise specified*

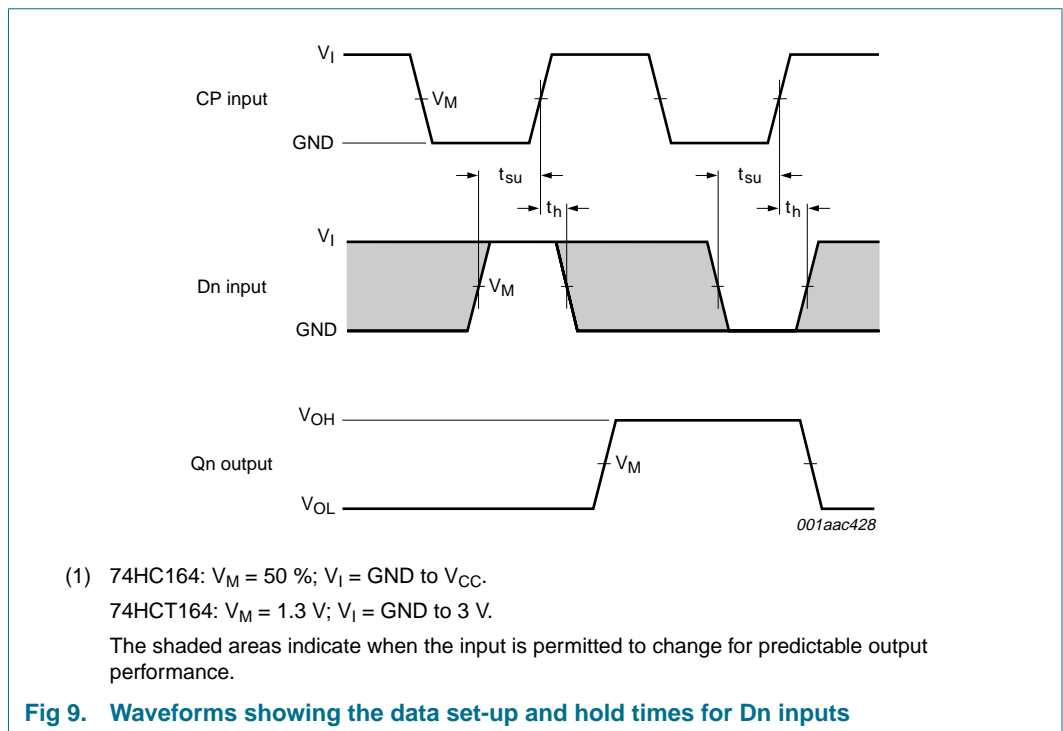
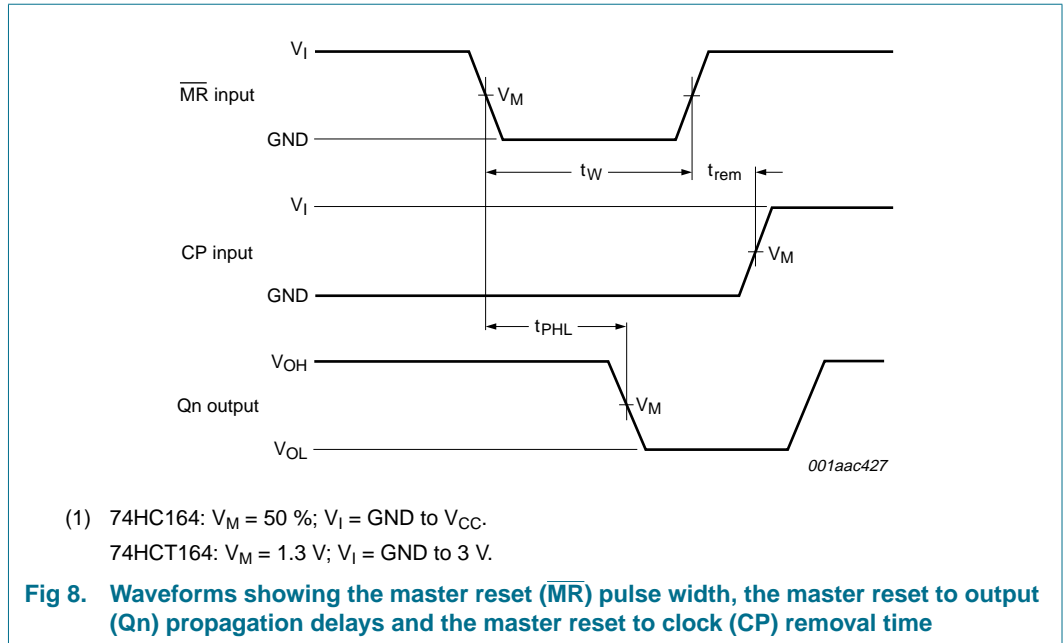
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
t_{PHL}, t_{PLH}	propagation delay CP to Qn	$V_{CC} = 4.5$ V; see Figure 7	-	17	36	ns
t_{PHL}	propagation delay \overline{MR} to Qn	$V_{CC} = 4.5$ V; see Figure 8	-	19	38	ns
t_{THL}, t_{TLH}	output transition time	$V_{CC} = 4.5$ V; see Figure 7	-	7	15	ns
t_W	clock pulse width; HIGH or LOW	$V_{CC} = 4.5$ V; see Figure 7	18	7	-	ns
	master reset pulse width; LOW	$V_{CC} = 4.5$ V; see Figure 8	18	10	-	ns
t_{rem}	removal time \overline{MR} to CP	$V_{CC} = 4.5$ V; see Figure 8	16	7	-	ns
t_{su}	set-up time DSA, and DSB to CP	$V_{CC} = 4.5$ V; see Figure 9	12	6	-	ns
t_h	hold time DSA, and DSB to CP	$V_{CC} = 4.5$ V; see Figure 9	+4	-2	-	ns
f_{max}	maximum clock pulse frequency	$V_{CC} = 4.5$ V; see Figure 7	27	55	-	MHz
$T_{amb} = -40$ °C to +85 °C						
t_{PHL}, t_{PLH}	propagation delay CP to Qn	$V_{CC} = 4.5$ V; see Figure 7	-	-	45	ns
t_{PHL}	propagation delay \overline{MR} to Qn	$V_{CC} = 4.5$ V; see Figure 8	-	-	48	ns
t_{THL}, t_{TLH}	output transition time	$V_{CC} = 4.5$ V; see Figure 7	-	-	19	ns
t_W	clock pulse width; HIGH or LOW	$V_{CC} = 4.5$ V; see Figure 7	23	-	-	ns
	master reset pulse width; LOW	$V_{CC} = 4.5$ V; see Figure 8	23	-	-	ns
t_{rem}	removal time \overline{MR} to CP	$V_{CC} = 4.5$ V; see Figure 8	20	-	-	ns
t_{su}	set-up time DSA, and DSB to CP	$V_{CC} = 4.5$ V; see Figure 9	15	-	-	ns
t_h	hold time DSA, and DSB to CP	$V_{CC} = 4.5$ V; see Figure 9	4	-	-	ns
f_{max}	maximum clock pulse frequency	$V_{CC} = 4.5$ V; see Figure 7	22	-	-	MHz
$T_{amb} = -40$ °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay CP to Qn	$V_{CC} = 4.5$ V; see Figure 7	-	-	54	ns
t_{PHL}	propagation delay \overline{MR} to Qn	$V_{CC} = 4.5$ V; see Figure 8	-	-	57	ns
t_{THL}, t_{TLH}	output transition time	$V_{CC} = 4.5$ V; see Figure 7	-	-	22	ns

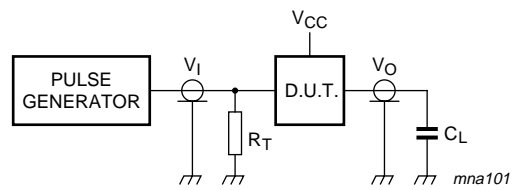
Table 10: Dynamic characteristics for 74HCT164 ...continued

$GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; test circuit see [Figure 10](#); unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_w	clock pulse width; HIGH or LOW	$V_{CC} = 4.5\text{ V}$; see Figure 7	27	-	-	ns
	master reset pulse width; LOW	$V_{CC} = 4.5\text{ V}$; see Figure 8	27	-	-	ns
t_{rem}	removal time \overline{MR} to CP	$V_{CC} = 4.5\text{ V}$; see Figure 8	24	-	-	ns
t_{su}	set-up time DSA and DSB to CP	$V_{CC} = 4.5\text{ V}$; see Figure 9	18	-	-	ns
t_h	hold time DSA and DSB to CP	$V_{CC} = 4.5\text{ V}$; see Figure 9	4	-	-	ns
f_{max}	maximum clock pulse frequency	$V_{CC} = 4.5\text{ V}$; see Figure 7	18	-	-	MHz







Definitions test circuit.

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig 10. Load circuitry for switching times

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

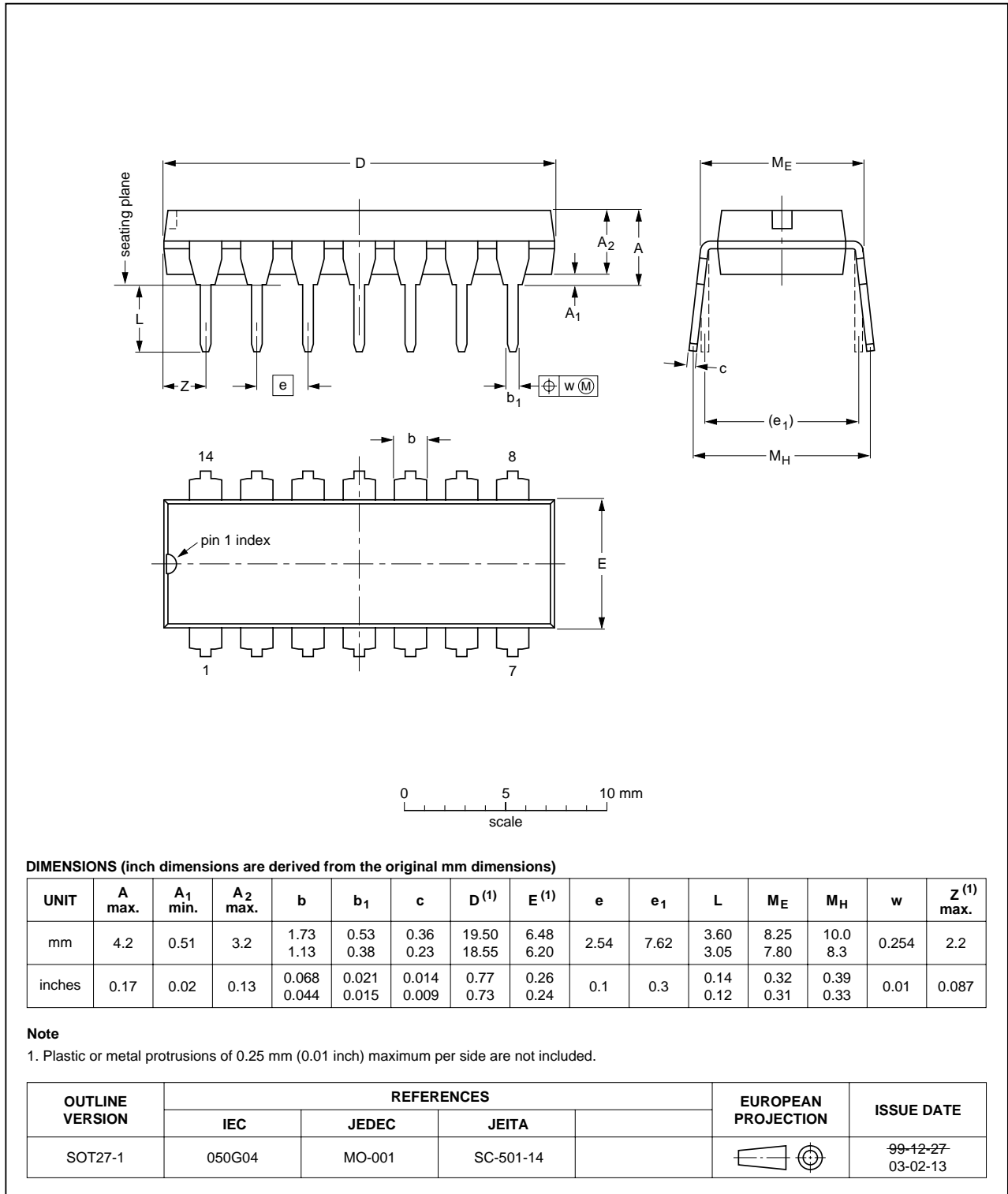


Fig 11. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm; body thickness 1.47 mm

SOT108-2

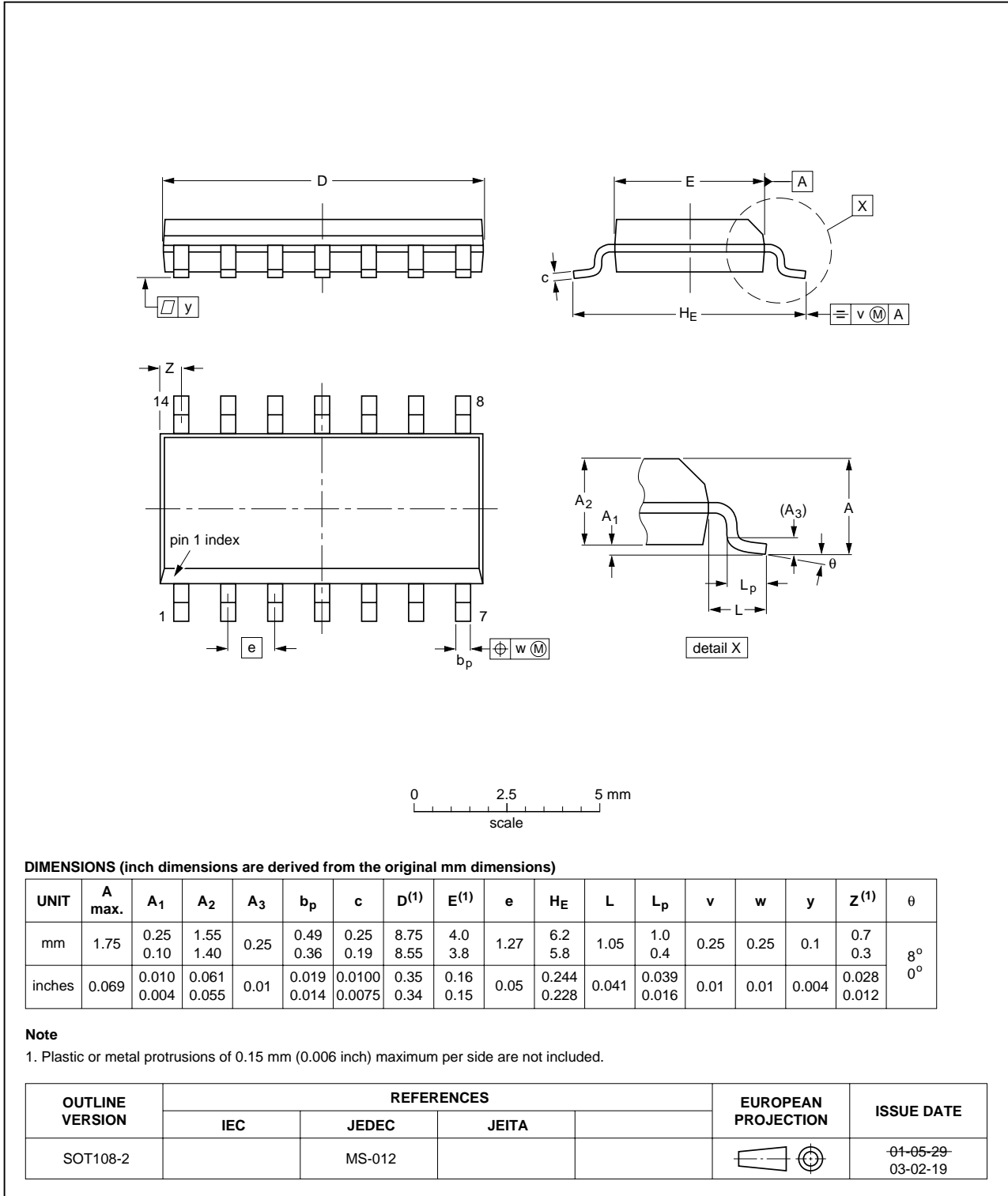


Fig 12. Package outline SOT108-2 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

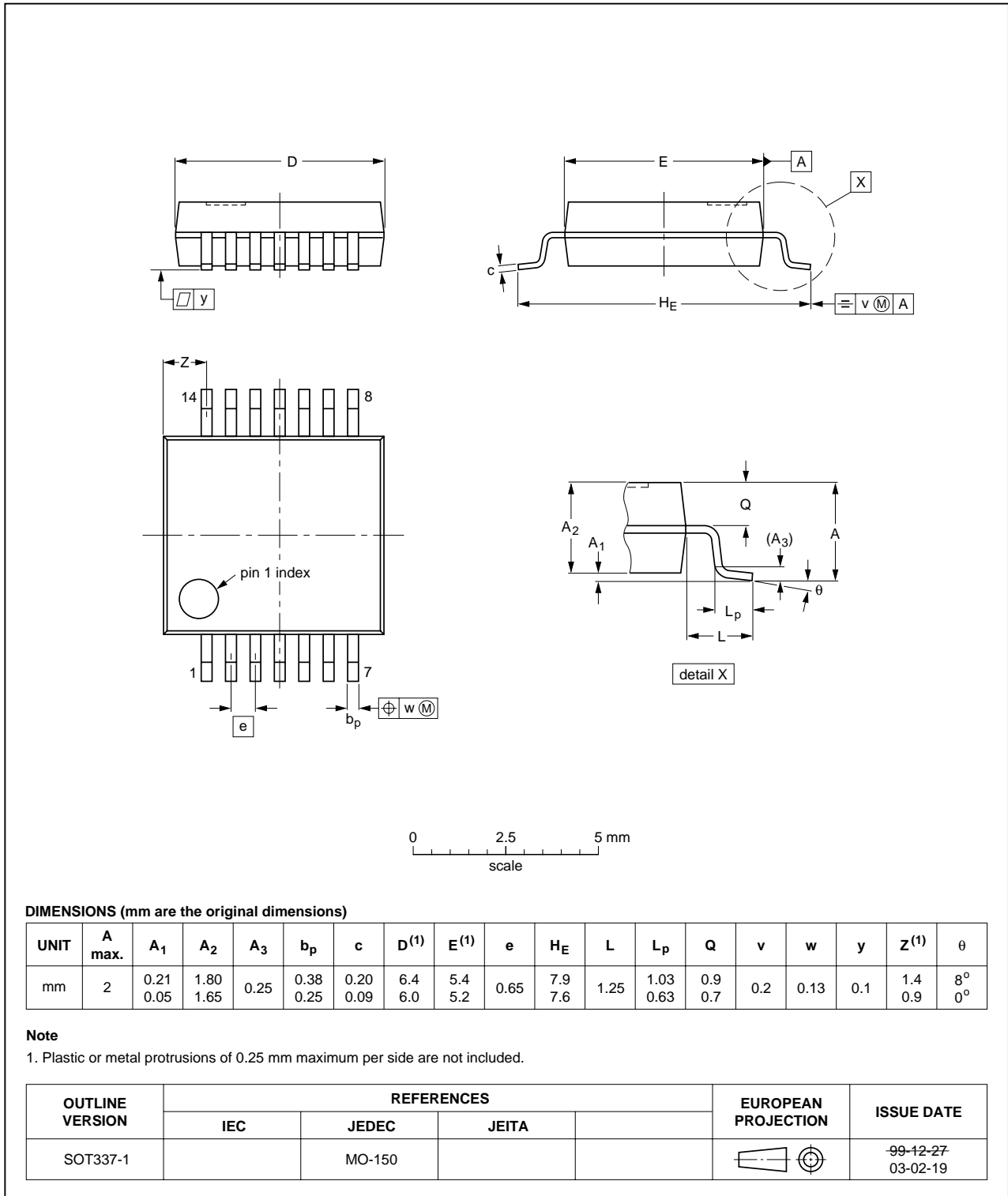


Fig 13. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

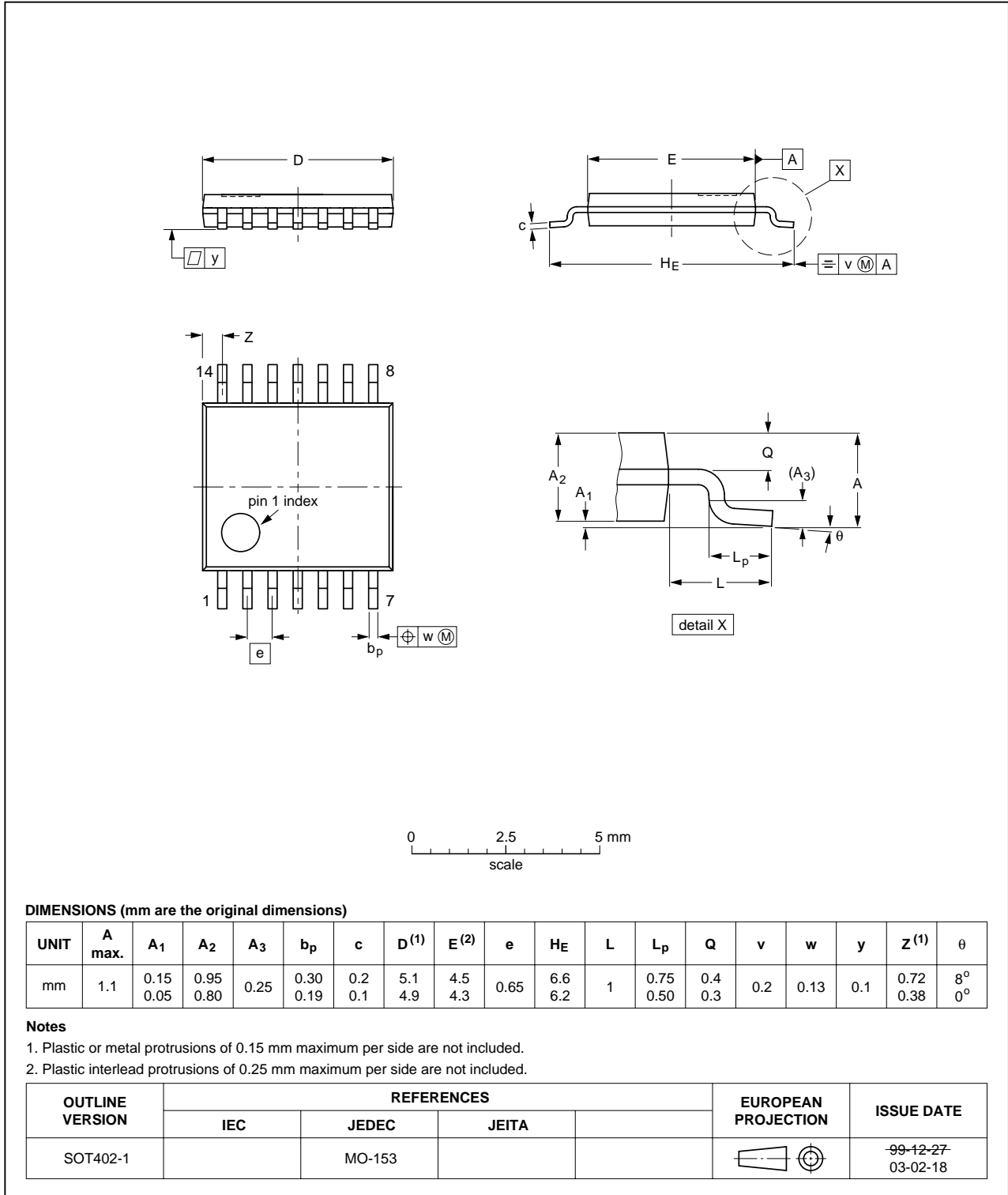


Fig 14. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

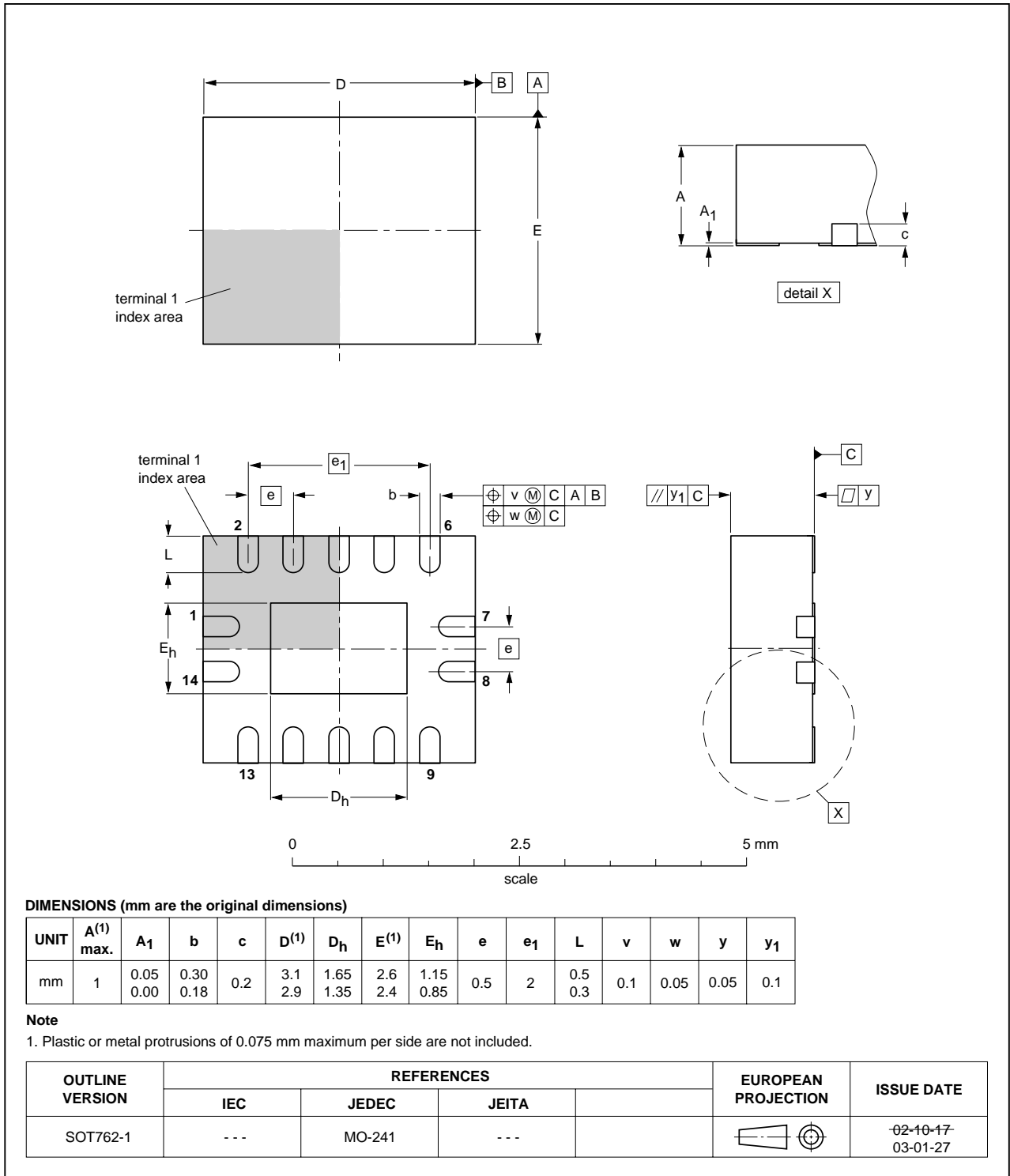


Fig 15. Package outline SOT762-1 (DHVQFN14)

13. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HC_HCT164_3	20050404	Product data sheet	-	9397 750 14693	74HC_HCT164_CNV_2
Modifications:					
			<ul style="list-style-type: none">• The format of this data sheet is redesigned to comply with the current presentation and information standard of Philips Semiconductors• Added SOT762-1 and Ordering information		
74HC_HCT164_CNV_2	19901201	Product specification	-	-	-

14. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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